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**Code No.: 6122 M**

# VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

**M.E. I Year (ECE) I-Semester (Make Up) Examinations, March-2016**

**(Embedded Systems & VLSI Design)**

## Digital IC Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** questions from **Part-B***

***Part-A (10 X 2=20 Marks)***

1. Define clock skew. How does it affect the performance of a VLSI system?
2. How does the VTC of a CMOS inverter change if the NMOS transistor is made stronger?
3. Compare and contrast both CMOS and pseudo-NMOS inverters. Draw their VTCs.
4. Estimate the intrinsic time constant of a balanced CMOS inverter.
5. Distinguish between a latch and a register with the help of a timing diagram.
6. Give the Elmore delay model for a 1 mm long interconnect split into 10 sections.
7. How does pipelining reduce power consumption in VLSI systems?
8. Draw a level restorer circuit and explain its working.
9. Why is a pre-decoder necessary for decoding Row address in SRAM structures?
10. Compare a 1T DRAM cell with a 6T SRAM cell with the help of circuit diagrams.

***Part-B (5 × 10 = 50 Marks)***

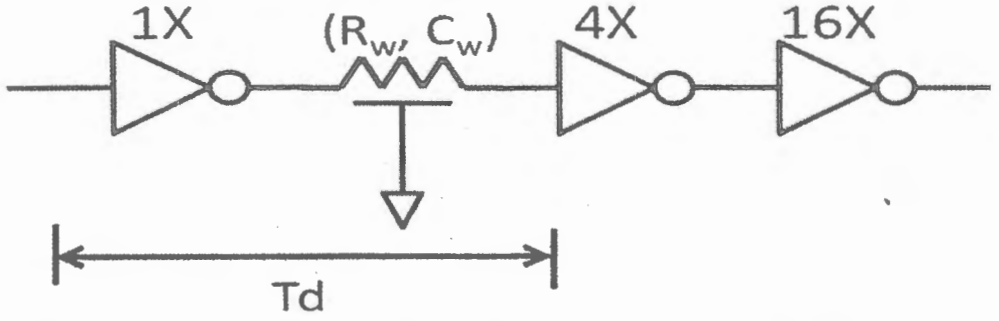
***(All bits carry equal marks)***

11. a) Compute the propagation delay, $t_{pd}$ of a CMOS inverter in 0.25 μ technology. Plot the $t_{pd}$ as a function of β and interpret the effect of sizing on propagation delay.

    b) Design a pseudo-NMOS inverter for $V_{OL} = 0.2V$ and $t_{pHL} \leq 100$ ps. Assume $C_L = 50$ fF.

12. a) Implement XOR/XNOR functions using CMOS and CPL gates and compare their performance.

    b) An FO4 inverter chain is shown below. The first and second stages are connected by a 100 μ x 0.25 μ long poly wire. Calculate the $T_{dLH}$ and $T_{dHL}$ using 0.25μ technology parameters. Assume $R_W = 150\ \Omega/\square$, $C_W = 0.1$ fF/μ$^2$, $R_{NMOS} = 10K$ and $R_{PMOS} = 12K$ for a unit size inverter.




13. a) Give the schematic of a CMOS Dual Edge Triggered (DET) Register and show that its throughput is twice that of an edge triggered register. What is the trade off?

    b) What are the challenges in distributing power and clock in a VLSI system? Give two clock distribution techniques followed in VLSI system design.

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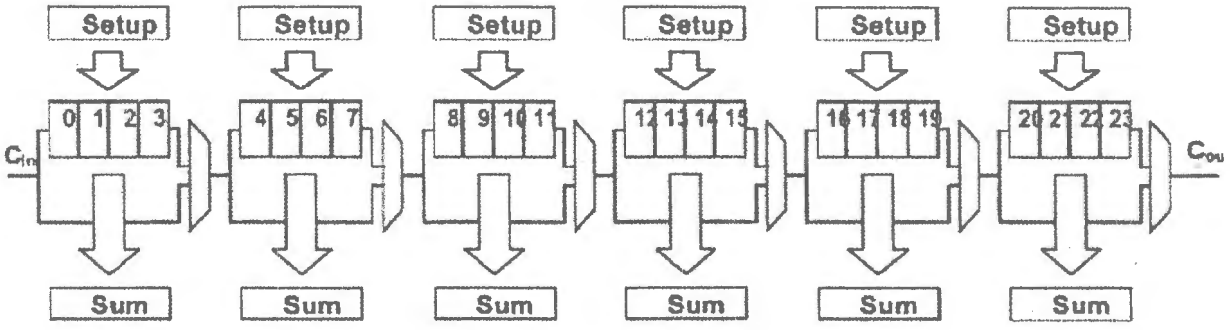
14. a) Explain the working principle of a 4 bit Manchester Carry chain adder and find its critical path delay. What are its limitations? How do you overcome them?

    b) A 24 bit, 6 stage Carry Bypass adder with $t_{setup}$ = 4ns, $t_{carry}$ =1ns, $t_{sum}$ =4ns and $t_{bypass}$ = 2ns is given below. Identify the critical path and list the delays for each block along the critical path. Find the total delay assuming each stage bypasses the same number of bits.

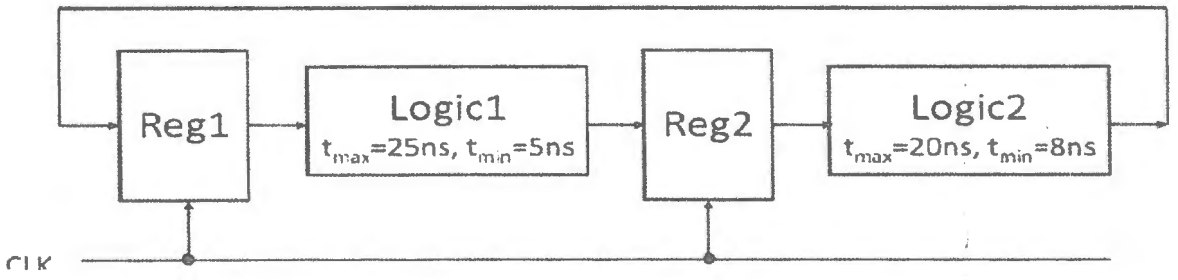



15. a) Draw the circuit of a 3T DRAM cell and explain its Read/ write operations with the help of timing diagrams.

    b) What is Memory Yield? What are the challenges and techniques in DSM regime for improving Memory Yield?

16. a) Show that for a balanced CMOS inverter $NM_L = NM_H$ and $t_{pHL} = t_{pLH}$.

    b) A pipelined system is shown below. Estimate the maximum frequency of operation of the system if there is no skew. Given $t_{CLK\text{-}Qmax}$ = 4 ns, $t_{CLK\text{-}Qmin}$ = 2 ns and $t_{setup} = t_{hold}$ = 1 ns, also estimate the maximum clock skew that the system can tolerate.




17. Write short notes on any **two** of the following:

    a) CMOS Schmitt Trigger

    b) Sense Amplifier Latch for SRAMs

    c) Power Management in VLSI Systems

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